REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1-24 are pending in the present application. Claims 1, 4, 8, 9, 12, 16, 17, 20, and 24 have been amended. Claims 6, 7, 14, 15, 22, and 23 have been cancelled.

II. Claim Amendments

Independent claims 1, 9, and 17 have been amended to recite that a circuit reduction method comprises inputting information about an original circuit structure; selectively sorting at least one node in the original circuit structure dependent on a resistive degree of the at least one node; dependent on the selectively sorting, determining at least one time constant of the at least one node; sorting the at least one time constant; and maintaining the at least one time constant from substantially all directions of the at least one node by redistributing at least one of a resistance and a ground capacitance, wherein the redistributing comprises eliminating another node having an insignificant characteristic time constant based on a local circuit transformation. No new matter has been added way of these amendments as support for these amendments may be found, for example, in original claims 1, 9, and 17 of the present application, Figure 3 of the present application, and paragraph [0021] of the present application.

Dependent claims 4, 12, and 20 have been amended to recite that the circuit

reduction method further comprises determining another time constant of the original circuit after redistributing; sorting the another time constant; and determining whether to remove a loop in the original circuit structure based on the sorted another time constant and the sorted at least one node. No new matter has been added way of these amendments as support these amendments may be found, for example, in original claims 4, 12, and 20 of the present application.

Dependent claims 8, 16, and 24 have been amended to recite that the at least one time constant referred to in amended independent claims 1, 9, and 17, respectively, is an Elmore time constant. No new matter has been by way of these amendments as support for these amendments may be found, for example, in paragraph [0021] of the present application.

III. Objection(s) to the Drawings

The drawings were objected to under 37 CFR 1.83(a) as not showing every feature of the invention as specified in the claims. Specifically, the Examiner asserted that the claimed features of a resistive degree and how the sorting node and time constants are affected must be shown in the claims of the present application or cancelled from the claims of the present application.

With respect to language in the claims of the present application referring to "resistive degree," Figure 3 of the present application shows a step (**ST 44**) for a resistive degree sort. *See* Specification, paragraph [0019]. It is well known in the art that a resistive degree of a node is in reference to the resistances of other nodes. Therefore, a node having high resistance has a higher resistive degree than a node having low

resistance.

With respect to language in the claims of the present application referring to the sorting of "nodes" and "time constants," Figure 3 of the present application shows steps (**ST 44** and **ST 48**) for sorting nodes based on their respective resistive degrees and time constants. *See* Specification, paragraphs [0019] and [0020]. Each node has an associated resistance and time constant, and depending on the relative values of the associated resistance and time constant to that of other nodes, the node is sorted.

Accordingly, withdrawal of the objections to the drawings is respectfully requested.

IV. Rejection(s) Under 35 U.S.C § 112

Claims 1-24 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. For the reasons set forth below, this rejection is respectfully traversed.

Claims 1, 9, and 17 of the present application were rejected as not being enabled by a description of a resistive degree in the Specification of the present application. In view of this assertion, Applicant notes that paragraph [0019] of the Specification, in reference to Figure 3 of the present application, states that "one or more nodes of the original circuit are sorted based on resistive degrees of the one or more node[s]." It would be obvious to one of ordinary skill in the art that this statement means that nodes are sorted based on their associated resistances in relation to the associated resistances of other nodes. For example, as explained above, a node having high resistance has a higher resistive degree than a node having low resistance. Thus, the language in the claims of

the present application referring to "resistive degree" is supported and enabled by the Specification of the present application.

Claims 1, 4, 9, 12, 17, and 20 of the present application were rejected as not being enabled by a description of the sorting of "nodes" and "time constants" in the Specification of the present application. In view of this assertion, Applicant notes that paragraphs [0019] and [0020] of the Specification, in reference to Figure 3 of the present application, state that "one or more nodes of the original circuit are sorted based on resistive degrees of the one or more node[s]" and "the time constants [of the one or more nodes] are evaluated and sorted." It would be obvious to one of ordinary skill in the art that these statements mean that nodes are sorted based on their resistive degrees as discussed above and time constants. For example, a particular node may be sorted according to a comparison of its resistance and time constant to a resistance and a time constant of another node. Thus, the language in the claims of the present application referring to the sorting of "nodes" and "time constants" is supported and enabled by the Specification of the present application.

Accordingly, withdrawal of the § 112, first paragraph, rejection of claims 1-24 of the present application is respectfully requested.

V. Rejection(s) Under 35 U.S.C § 102

Claims 1-5, 8-13, 16-21, and 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by the cited referenced authored by Sheehan and entitled "TICER: Realizable Reduction of Extracted RC Circuits" (reference hereinafter as "Sheehan"). For the reasons set forth below, this rejection is respectfully traversed.

Applicant notes that the Examiner did not reject original, now cancelled, claims 6, 7, 14, 15, 22, and 23 of the present application over Sheehan. To the extent that the limitations of these claims have now been respectively incorporated into amended independent claims 1, 9, and 17 of the present application, the rejection over Sheehan is moot.

However, to the extent that Sheehan may still apply to amended independent claims 1, 9, and 17 of the present application, Applicant submits the following remarks. The present invention is directed to a technique for generating a netlist that maintains a topology of an original circuit while preserving the original circuit's functions and characteristics. The technique, as recited in amended independent claims 1, 9, and 17 of the present application, requires: inputting information about an original circuit structure; selectively sorting at least one node in the original circuit structure dependent on a resistive degree of the at least one node; dependent on the selectively sorting, determining at least one time constant of the at least one node; sorting the at least one time constant; and maintaining the at least one time constant from substantially all directions of the at least one node by redistributing at least one of a resistance and a ground capacitance, wherein the redistributing comprises eliminating another node having an insignificant characteristic time constant based on a local circuit transformation.

Sheehan, in contrast to the present invention, fails to disclose the arrangement recited in amended independent claims 1, 9, and 17 of the present application. For example, Sheehan discloses a technique for eliminating nodes based on their time constants, but fails to disclose, either expressly or impliedly, redistributing at least one of a resistance and a ground capacitance (Sheehan positions new resistors/resistances

determined using equations that do not facilitate the redistribution of resistors/resistances of an original circuit) by eliminating a node having an insignificant characteristic time constant based on a local circuit transformation (Sheehan does not consider the time constant of a node based on a local circuit transformation), where the redistributing occurs in such as manner as to maintain the time constant of a node of interest from substantially all directions (not merely two directions as disclosed by Sheehan).

In view of the above, Sheehan fails to show or suggest the present invention as recited in amended independent claims 1, 9, and 17 of the present application. Thus, amended independent claims 1, 9, and 17 of the present application are patentable over Sheehan. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

VI. Conclusion

Applicant believes this reply to be fully responsive to all outstanding issues and place this application in condition for allowance. If this belief is incorrect, or other issues arise, do not hesitate to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.101001;P5978).

Respectfully submitted,

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